Application Note 46
Special Features of RCC700A

This application note is intended to explain the special features of RCC700A.

CSEL

RCC700A has the capability to disable the 8b/10b encoder/decoder by applying a "1" to the CSEL pin. This allows the RCC700A to be used when the 8b/10b encoder/decoder functions are available on another chip.

Byte Sync Enable

RCC700A has a pin called SYNCEN. Normally, this pin can be asserted HIGH and remain HIGH. Under marginal link conditions, in order to make sure that the receiver does not align to a false K28.5, this pin can be deasserted once the byte synchronization has taken place. This will ensure that there is no false alignment.

Reset

The reset function is provided to reset the transmit and receive Phase Locked Loop (PLL) present within the chip. For RCC700A, the reset pin, RST is an active HIGH signal for CSEL = 0. When asserted for at least one byte clock, it resets both of the PLLs. This feature is not normally needed. Only under extraordinary circumstances of the PLLs being out of lock do we need to assert this function. The PLL designed in RCC700A is resilient to noise and quiet conditions at the receive input. The reset function is active LOW for CSEL = 1.

Polarity Select (CSEL =1 only)

In RCC700A, Polarity Select for the receive byte clock (RBC) is provided by means of a pin POLSEL. When POLSEL is HIGH, the receive output data, DO0...DO9 is centered with respect to the negative edge of RBC. This is useful to comply with the Optical Link Card (OLC) requirements in Fibre Channel applications. For other applications, this pin can remain floating or connected to ground. Under that case, the receiver output, DO0..DO9, is centered with respect to the positive edge of RBC.

Transmit Output LOW

RCC700A has the means to force the transmit serial output LOW when the device is not transmitting by means of asserting DOL pin HIGH. This feature is useful in fiber applications when the device is connected to the fiber through a fiber optic transceiver module. When the chip is not transmitting any data, it can be forced to transmit LOW signal by asserting DOL HIGH. This will protect the fiber optic transmitter from continuous HIGH state conditions. When DOL is asserted HIGH, any data that is transmitted are ignored.

Parity (CSEL = 0 only)

RCC700A has the means to verify odd parity on the transmit portion and generate odd parity on the receive portion. This is useful to preserve the data integrity in data transfers to memory. The parity bit on the transmit is conveyed through PIN signal. If the odd parity of the data inputs, DI0..DI7, does not match that of PIN, the error condition is conveyed through a signal called PE. PE when HIGH indicates parity error. An example of odd parity is as follows: If DI0..DI7 is 01010000, the odd parity is 1. This is derived by counting the number of 1s in the input data and if it is even, then the parity is 1. Otherwise it is 0. In this example, the number of 1s was 2. Hence the odd parity is 1.

On the receive portion, odd parity is generated for the data outputs, DO0..DO7, through POUT signal.

BSYNC

For RCC700A, byte synchronization on the receive portion is conveyed through BSYNC signal. Whenever one of the three characters, K28.1, K28.5, or K28.7 are received, it is indicated through the BSYNC signal. The receiver provides byte alignment to any of these three characters.

LSEL

RCC700A can be put in the internal loopback state by means of asserting LSEL signal HIGH. This is useful for node diagnostics. When LSEL is asserted, the serial transmit data is also provided through DOUT, $\overline{\text{DOUT}}$. If DOL is asserted HIGH, it overrides any loopback conditions to provide LOW serial output.

Transmit Error (CSEL = 0 only)

RCC700A has the means to transmit an error through the serial output by means of forcing ETX signal HIGH. In this case, alternating 10 bit codes 1001111011, 0110000100 are sent. This is detected as invalid codes on the receiver. This is useful to check out the communicating link for diagnostic purposes.

Error Flag (CSEL = 0 only)

RCC700A verifies the received codes for conformance to 10b/8b decoding table and any invalid codes or invalid running disparity are flagged through an error flag pin, EF.

Signal Detect

RCC700A has the means of converting a psuedo ECL signal detect input to an active LOW CMOS output. This makes it easier for the system to interface the signal detect signal coming out of a fiber optic receiver.

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